

# The Research on Influencing Factors of 650 V IGBT's Turn-off $dV_{ce}/dt$ Controllability

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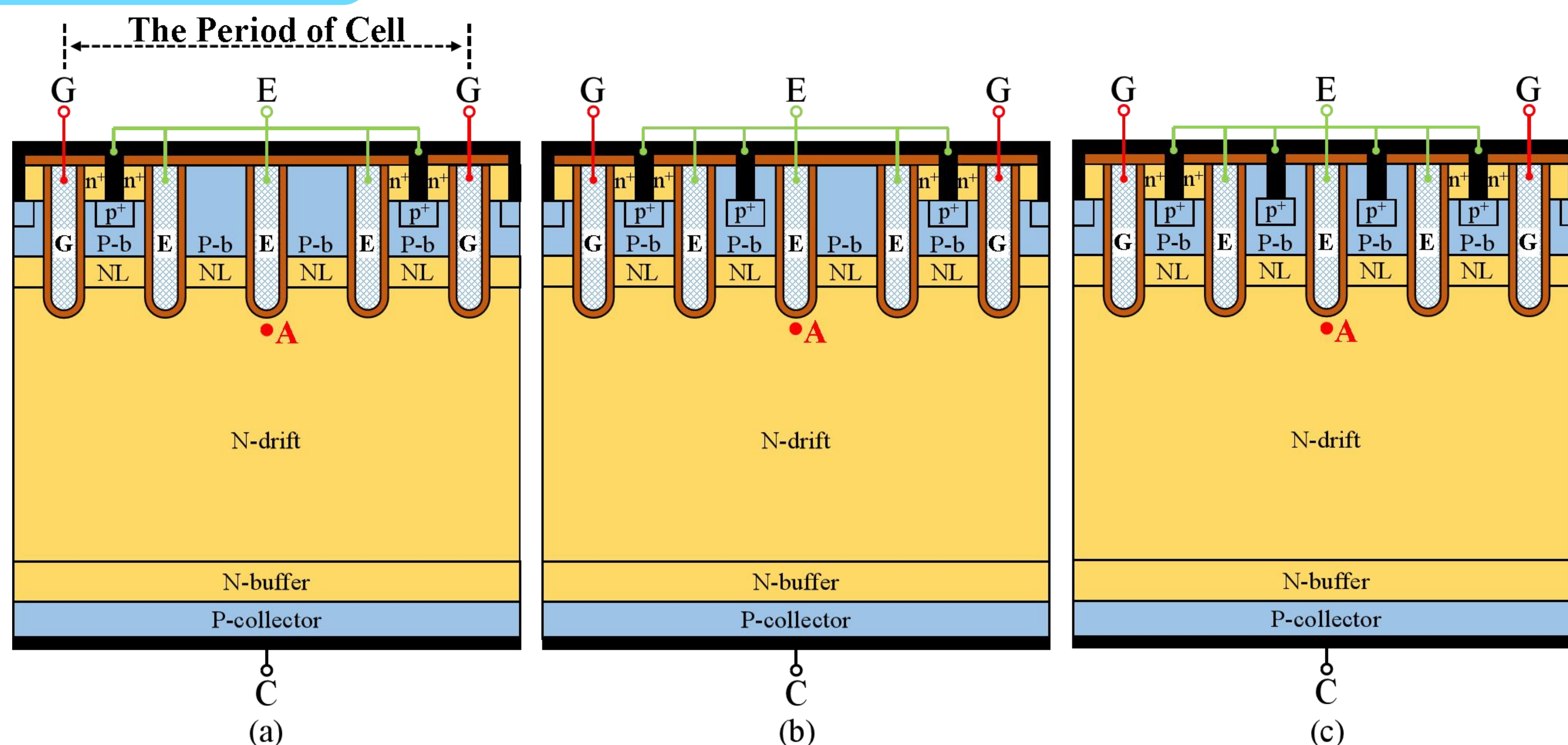
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## Introduction

The trench insulated gate bipolar transistor (IGBT) is an important switching device in power electronic applications. IGBTs are moving towards higher power density and operating frequency. However, during the switching phase, excessive current density and excessive  $dV_{ce}/dt$  can lead to dynamic avalanche. Through experimental tests and simulations, the factors affecting the controllability of turn-off  $dV_{ce}/dt$  were researched, including the front structure (FSTR) of IGBT, as well as the bus voltage ( $V_{BUS}$ ) and the load current ( $I_{load}$ ) in the application conditions.

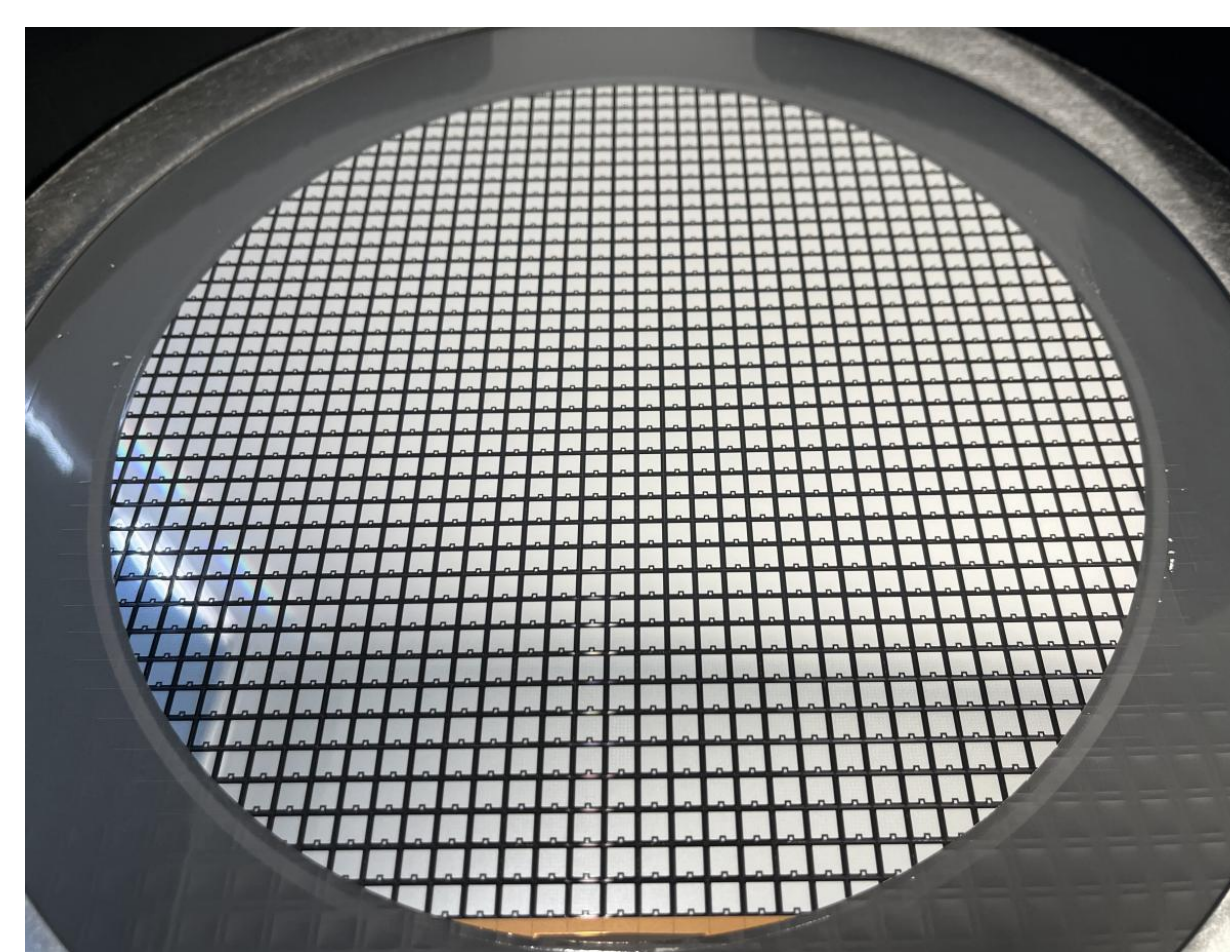
## Structure and Mechanism



**Fig. 1.** Schematic diagrams of IGBTs with different frontal structures: (a) FSTR-1, (b) FSTR-2 and (c) FSTR-3. The gate trench (GT) is connected to the  $V_g$  through the gate resistance ( $R_g$ ), and the emitter trench (ET) is shorted together with the emitter metal.

## Wafer appearance

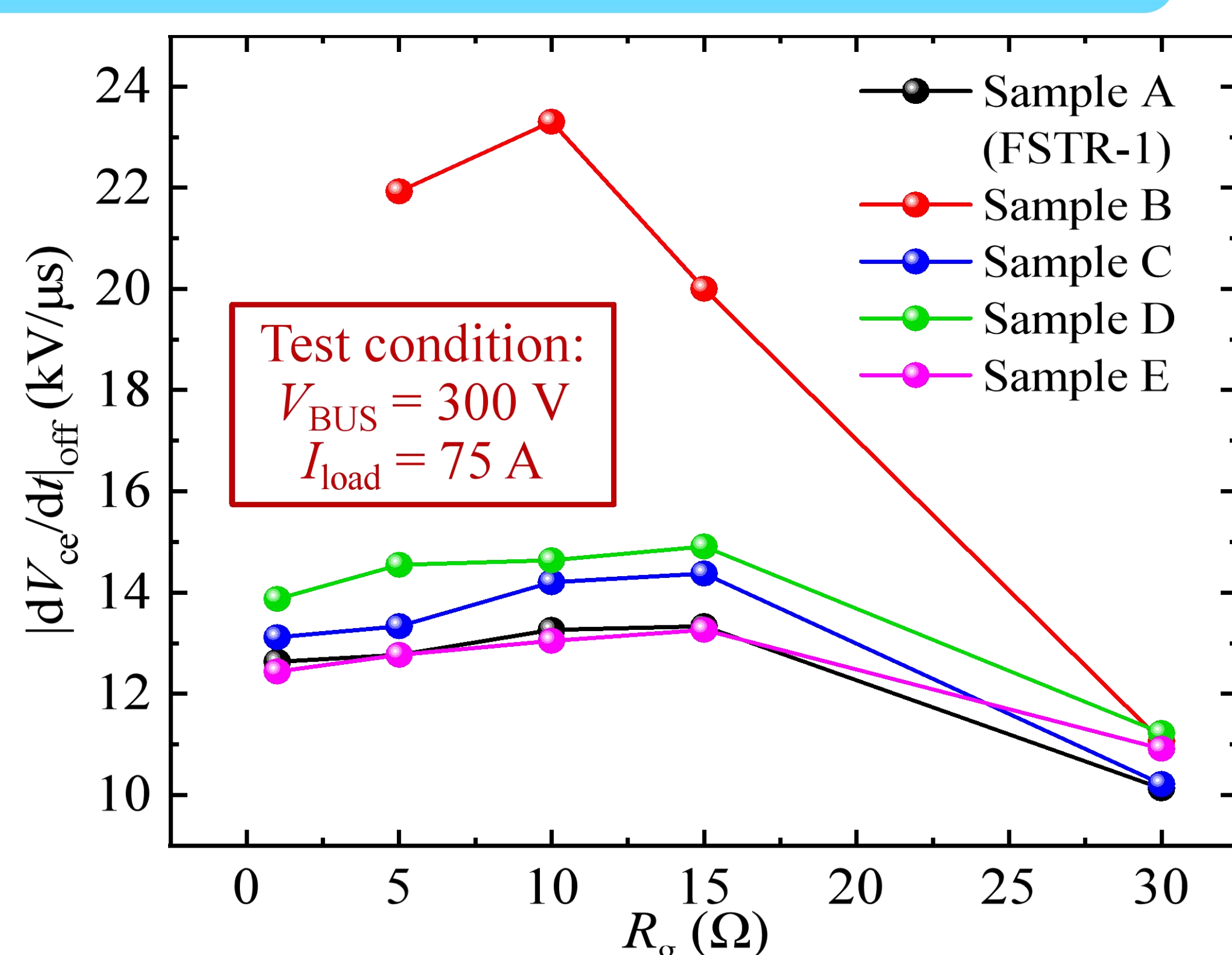
Adopted frontal structure 1 (FSTR-1)



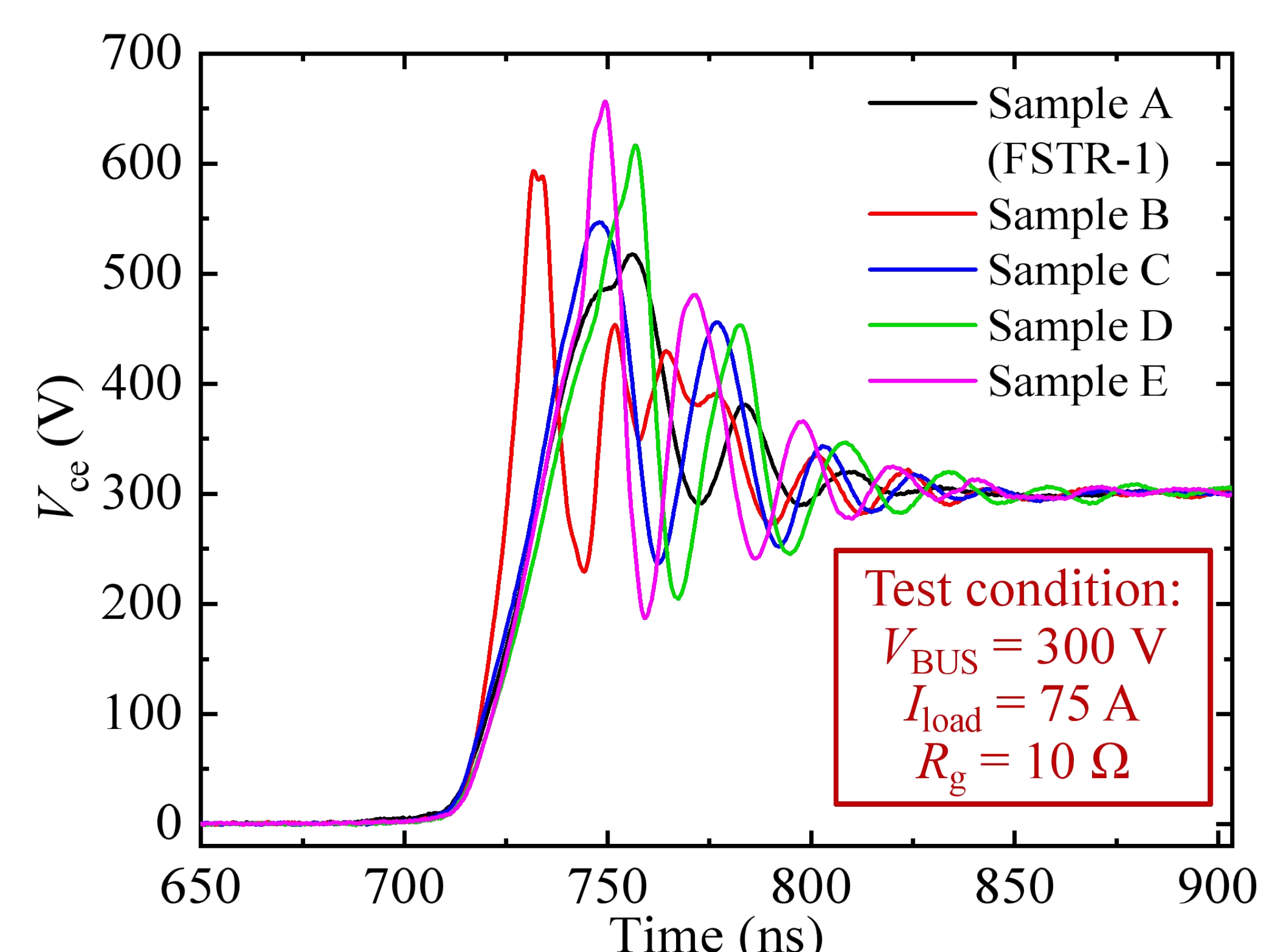
Size	Value
Wafer	8 inches
Chip	5 mm × 5 mm

**Fig. 2.** The chip appearance diagram of IGBT designed by adopted FSTR-1.

## Test Results of 650V-75A IGBT Samples



**Fig. 3.** The relationships between turn-off  $dV_{ce}/dt$  and  $R_g$  of different IGBT samples.



**Fig. 4.** The turn-off  $V_{ce}$  waveforms of different IGBT samples.

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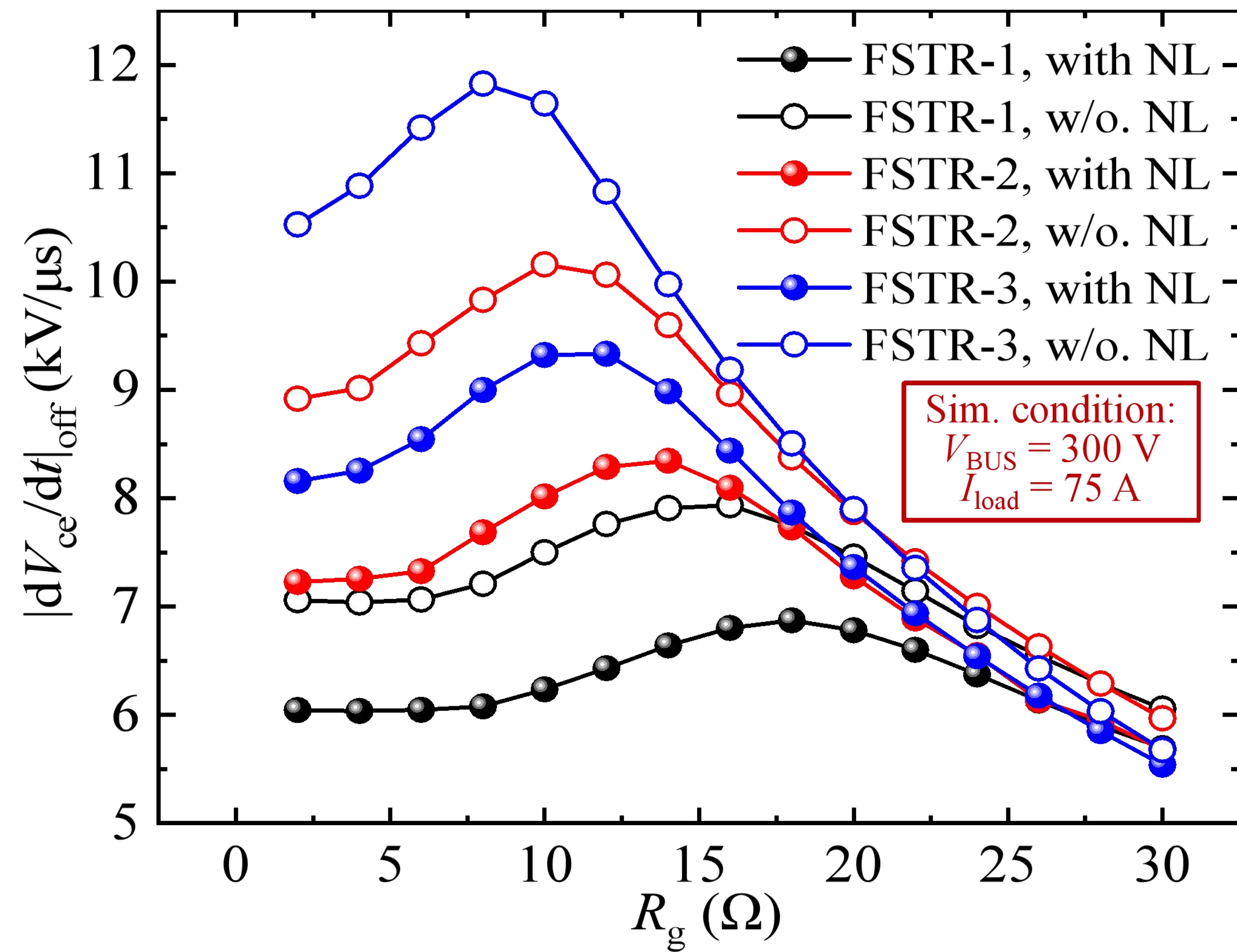
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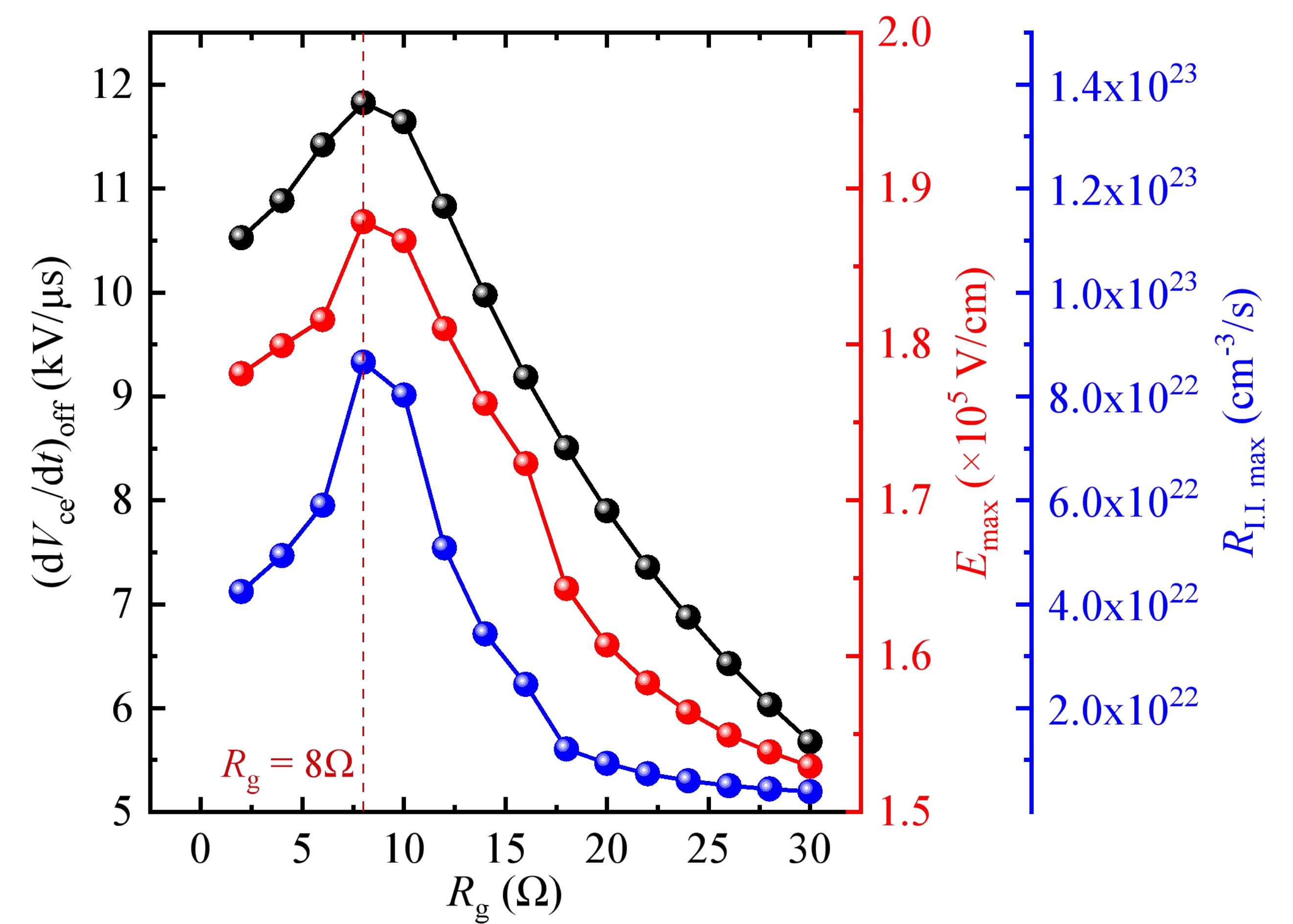
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## Simulation Results of Different FSTR



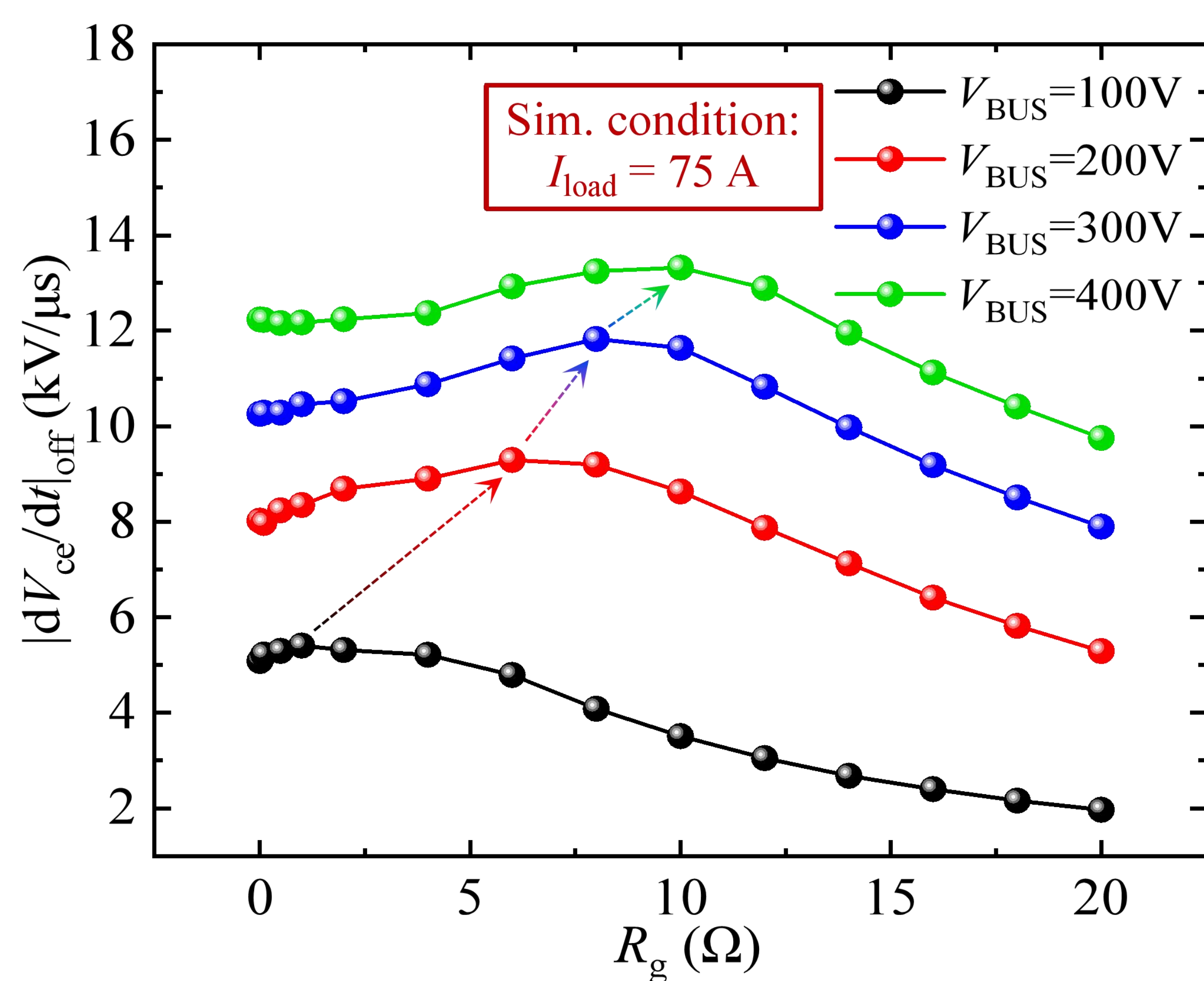
**Fig. 5.** The relationships between turn-off  $dV_{ce}/dt$  and  $R_g$  of different FSTRs.

## Analysis of phenomenas

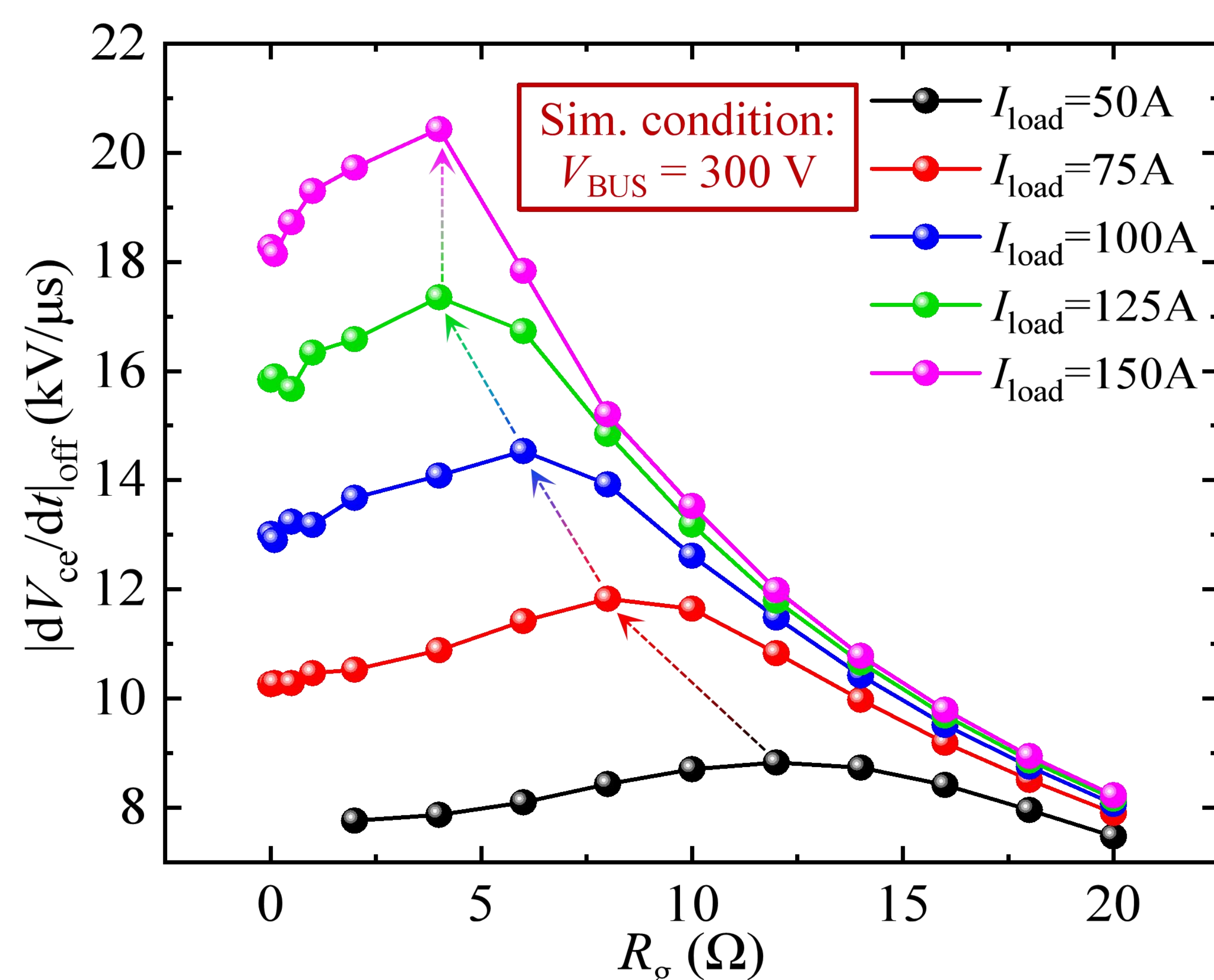


**Fig. 6.** Influence of  $R_g$  on  $E_{max}$  and  $R_{l,max}$  of point A in FSTR-3 without NL during turn-off period (at the moment the  $V_{ce}$  increases to 300V).

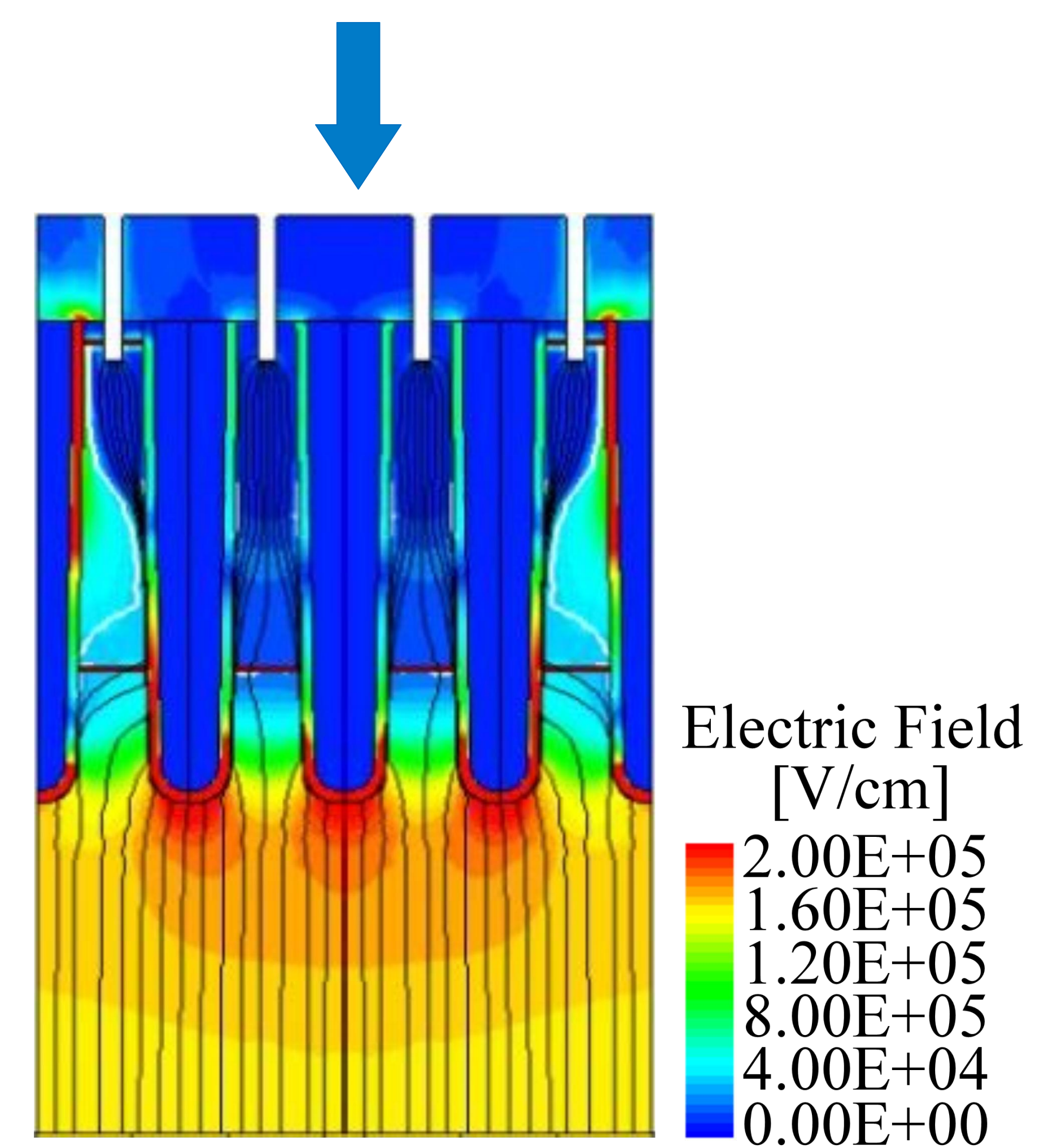
## Simulation Results of Different $V_{BUS}$ & $I_{load}$



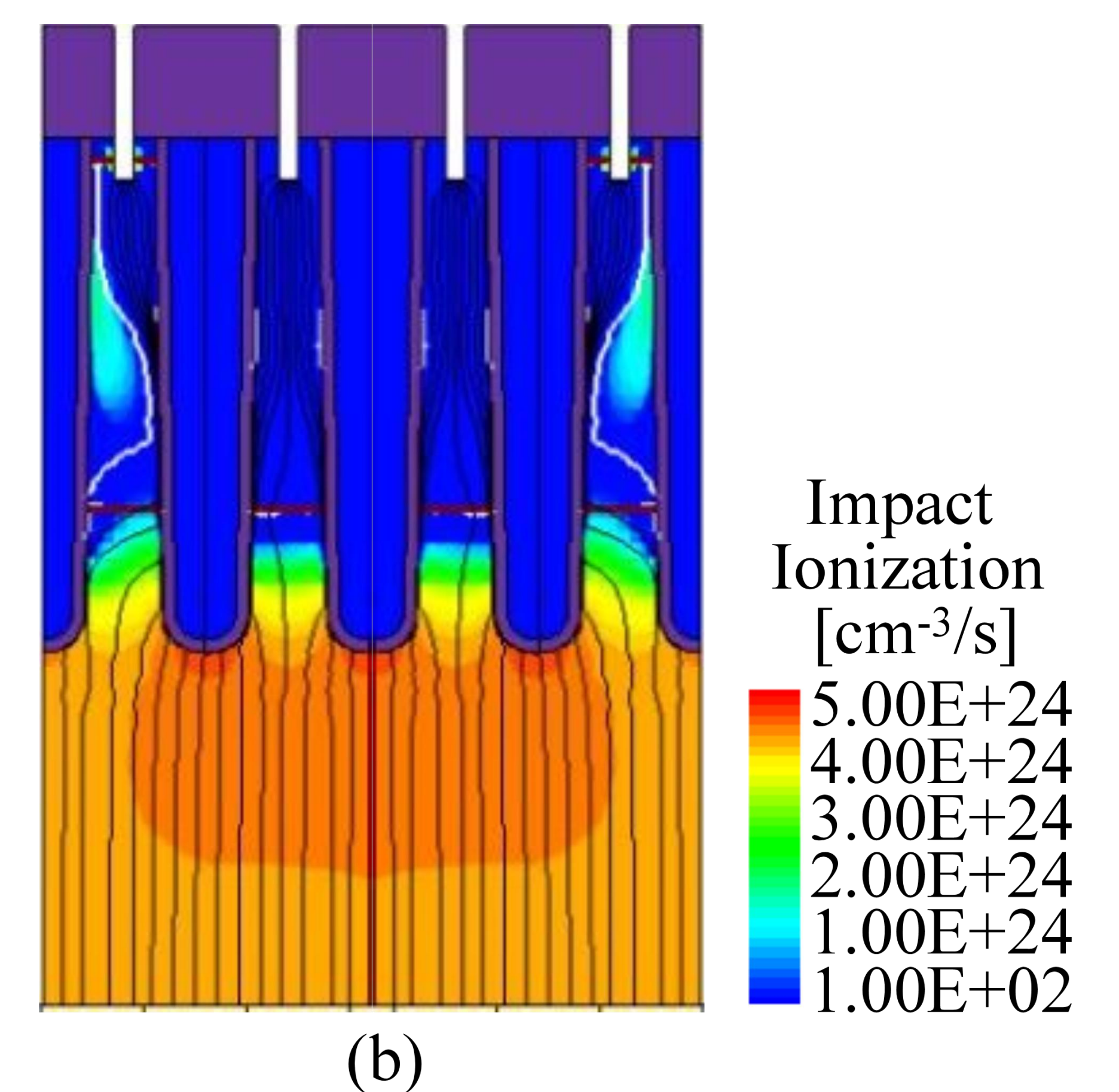
**Fig. 8.** The relationship between turn-off  $dV_{ce}/dt$  and  $R_g$  of different  $V_{BUS}$ .



**Fig. 9.** The relationship between turn-off  $dV_{ce}/dt$  and  $R_g$  of different  $I_{load}$ .



**Fig. 7. (a)** Distributions of electric field and current flow lines of FSTR-3 without NL when  $V_{ce}$  increase to 300 V during turn-off period.



**Fig. 7. (b)** Distributions of impact ionization rates and current flow lines of FSTR-3 without NL when  $V_{ce}$  increase to 300 V during turn-off period.